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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	
Gordon Ma et al.	§	Group Art Unit:
	§	
Serial No.:	§	Examiner:
	§	
Filing Date: **February 27, 2004**	§	
	§	
Title: **Semiconductor Structure**	§	Attny. Docket No. **068736.0236**
	§	Client Ref.: **2003P54948US**

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. A copy of the cited art is enclosed for the convenience of the Examiner.

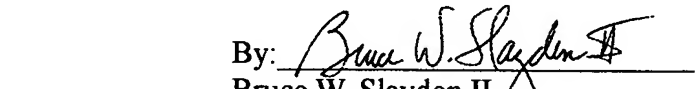
Furthermore, pursuant to 37 C.F.R. §§1.97(g) and (h), no representation is made that these references are material to the patentability of the present application.

As the Information Disclosure Statement is being submitted before the mailing of

the first office action on the merits, Applicants believe that no fee is required. If a fee is required, please accept this transmittal as a petition therefor and charge any fee to Baker Botts L.L.P. *(formerly, Baker & Botts, L.L.P.)* Deposit Account No. 02-0383, Order No. (***068736.0236***) for any other charges necessary for the filing of this Information Disclosure Statement.

BAKER BOTTS L.L.P. (023640)

Date: February 27, 2004

By: 

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Client Reference No. 068736.0236 PATENT

PTO-1449	Application No.	Applicant(s): GORDON MA ET AL.	
Information Disclosure Citation in an Application	Docket Number: 068736.0236	Group Art Unit	Filing Date: February 27, 2004

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	1	4,811,075	03/07/89	Eklund	357	46	04/24/87
	2	5,155,563	10/13/92	Davies et al.	357	23.4	03/18/91
	3	5,252,848	10/12/93	Adler et al.	257	328	02/03/92
	4	5,313,082	05/17/94	Eklund	257	262	02/16/93
	5	6,168,983	01/02/01	Rumennik et al.	438	188	02/05/99
	6	6,563,171	05/13/03	Disney	257	342	11/12/02

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	7	J.A. Appels and H.M.J. Vaes, "High voltage thin layer devices (RESURF devices)", IEDM technical digest, pp. 238-241	1979
	8	H.M.J. Vaes and J.A. Appels, "High voltage high current lateral devices", IEDM technical digest, pp. 87-90	1980
	9	T. Fujihira, "Theory of Semiconductor Superjunction Devices", Jpn. J. Appl. Phys., vol. 36, pp. pp. 6254-6262	1997
	10	G. Deboy, et al., "A new generation of high voltage MOSFETs breaks the limit line of silicon", IEDM technical digest, pp. 683-685	1998
	11	A. Ludikhuize, "A review of RESURF technology", Proc. of ISPSD, p. 11	2000
	12	J. Cai, et al., "A novel high performance stacked LDD RF LDMOSFET, IEEE Electron Device Lett., vol. 22, no. 5, pp. 236-238	2001
	13	J.G. Mena and C.A.T. Salama, "High voltage multiple-resistivity Drift-Region LDMOS", Solid State Electronics, Vol. 29, No. 6, pp. 647-656	1986
	14	M.D. Pocha and R.W. Dutton, "A computer-aided design model for High-Voltage Double Diffused MOS (DMOS) Transistors", IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 5	1976
	15	I. Yoshia, et al.; "Highly Efficient 1.5 GHz Si Power MOSFET for Digital Cellular Front End"; Proceedings of International Symposium on Power Semiconductor Devices & ICs; Tokyo, pp. 156-157	1992
	16	Helmut Brech et al; "Record Efficiency and Gain at 2.1 GHz of Hih Power RF Transistors for Cellular and 3G Base Stations"; RF & DSP INfrastructure Devision, Semiconductor Products Sector, Motorola, Tempe, Arizona	2003

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.